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**Abstract**

A clock synchronizer circuit provides an internal clock signal for an integrated circuit that is synchronized to an external system clock signal, such that the internal clock integrated is aligned with and has minimal skew from the external system clock signal. The clock synchronizer circuit allows synchronizing of internal clocks of an integrated circuit with the external system clock having a period  $\tau_{ck}$  less than the cumulative delay of internal receiving and distribution circuits of the integrated circuit.

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